Dual N-channel MOSFET

KFC6B22500L
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
for lithium-ion secondary battery protection circuits.

2. FEATURES

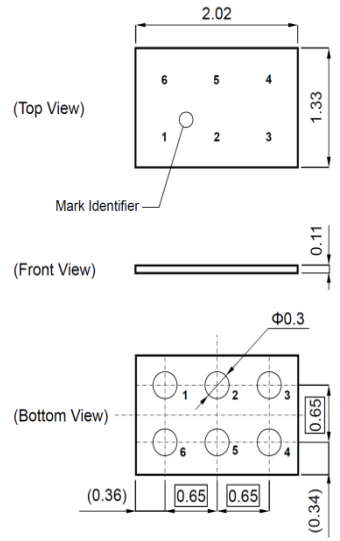
- Source-source On-state Resistance: RSS(on) typ = 8.3 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: 3S

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

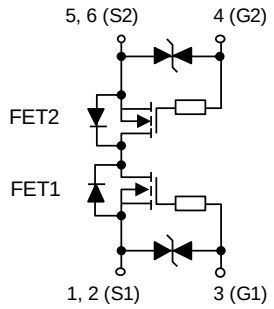
Unit: mm



1. Source1-1 (FET1) 4. Gate2 (FET2)
2. Source1-2 (FET1) 5. Source2-2 (FET2)
3. Gate1 (FET1) 6. Source2-1 (FET2)

Package	MLGA006-W-1320-RA
JEITA	-
Code	-

Equivalent circuit



5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	20	V
Gate-source Voltage		VGS	± 12	V
Source Current	DC *1	IS1	6.2	A
	DC *2	IS2	11.5	
	DC *3	IS3	14.5	
	Pulsed *4	ISp	62	
Total Power Dissipation	DC *1	PD1	0.44	W
	DC *2	PD2	1.5	
	DC *3	PD3	2.4	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	284	°C / W
	Rth2 *2	83	
	Rth3 *3	52	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (30 mm^2 area, 36 µm thickness).
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (610 mm^2 area, 36 µm thickness).
*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
*4 t = 10 µs, Duty Cycle ≤ 1 %.

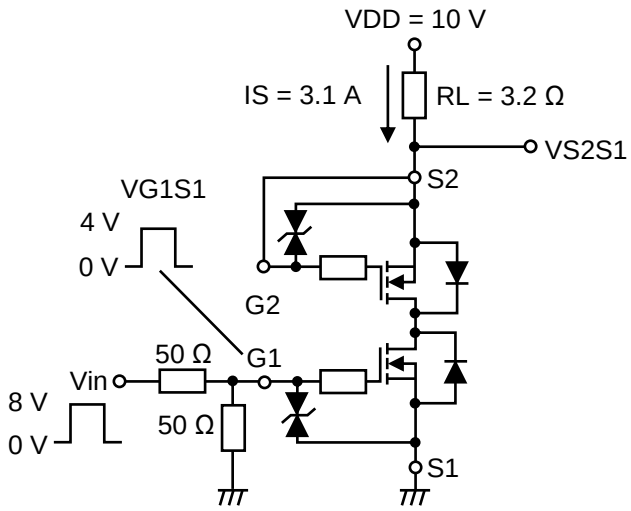
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

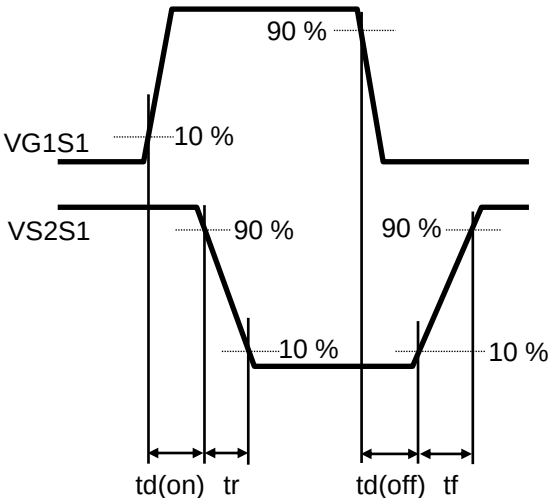
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	20			V
Zero Gate Voltage Source Current	ISSS	VSS = 20 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS1	VGS = ± 8 V, VSS = 0 V			± 10	μA
	IGSS2	VGS = ± 5 V, VSS = 0 V			± 1	
Gate-source Threshold Voltage	Vth	IS = 0.57 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 3.1 A, VGS = 4.5 V	5.2	7.9	10.3	mΩ
	RSS(on)2	IS = 3.1 A, VGS = 3.8 V	5.5	8.3	10.8	
	RSS(on)3	IS = 3.1 A, VGS = 3.1 V	5.8	9.2	14.7	
	RSS(on)4	IS = 3.1 A, VGS = 2.5 V	6.3	11.1	21.8	
Body Diode Forward Voltage	VF(s-s)	IF = 3.1 A, VGS = 0 V		0.7	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		1600		pF
Output Capacitance *1	Coss			165		
Reverse Transfer Capacitance *1	Crss			130		
Turn-on Delay Time *1, *2	td(on)	VDD = 10 V, VGS = 0 to 4 V		0.4		μs
Rise Time *1, *2	tr	IS = 3.1 A		0.9		
Turn-off Delay Time *1, *2	td(off)	VDD = 10 V, VGS = 4 to 0 V		2.1		μs
Fall Time *1, *2	tf	IS = 3.1 A		1.4		
Total Gate Charge *1	Qg	VDD = 10 V		13		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		5.2		
Gate-drain Charge *1	Qgd	IS = 6.2 A		4.0		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

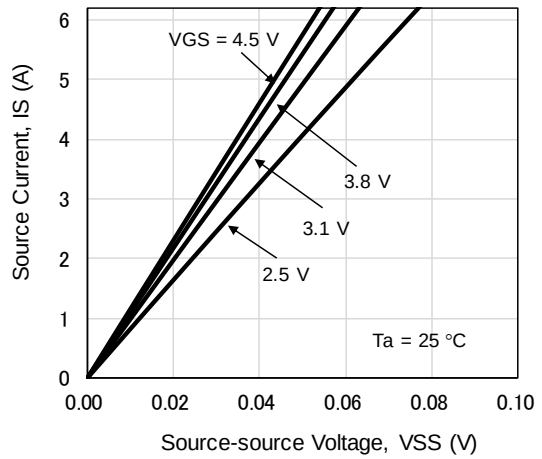
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



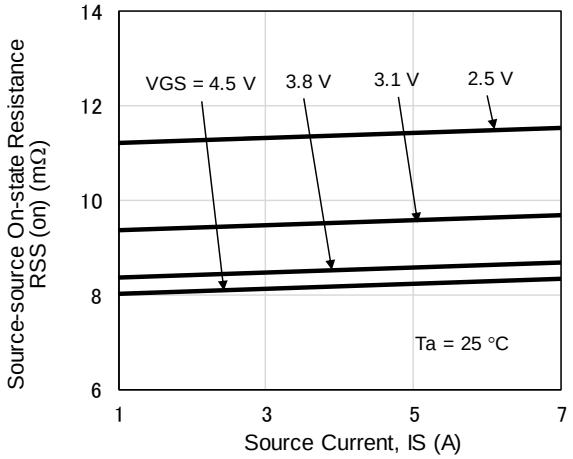


8. TECHNICAL DATA (Reference)

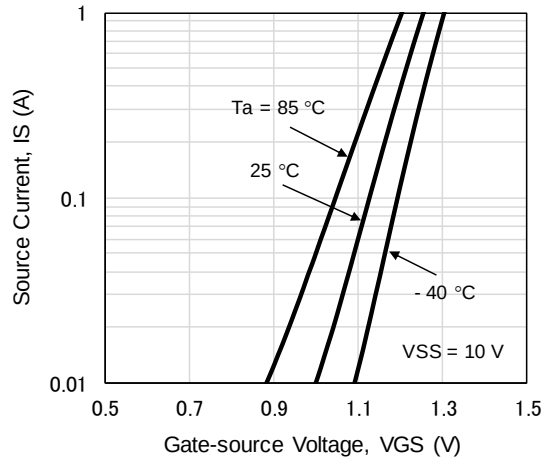
IS - VSS *1



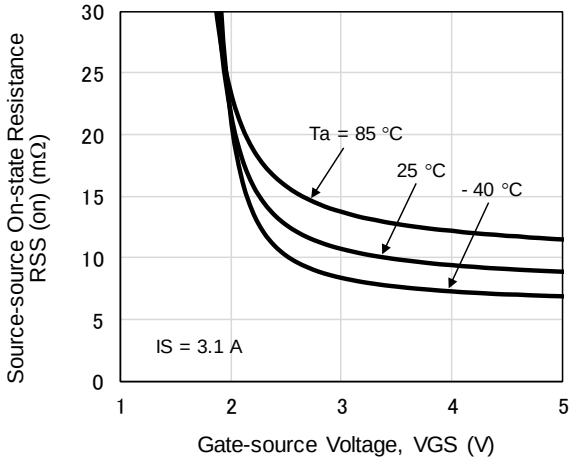
RSS(on) - IS *1



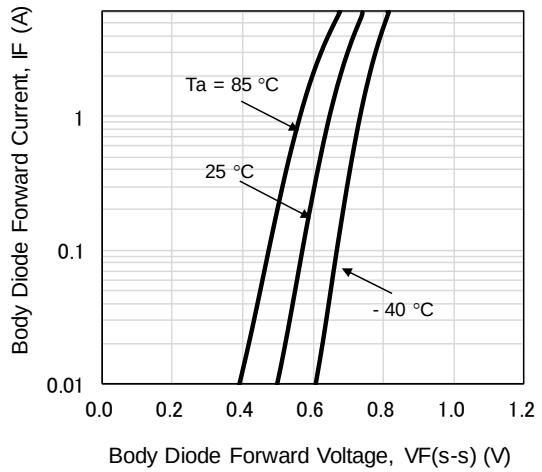
IS - VGS *1



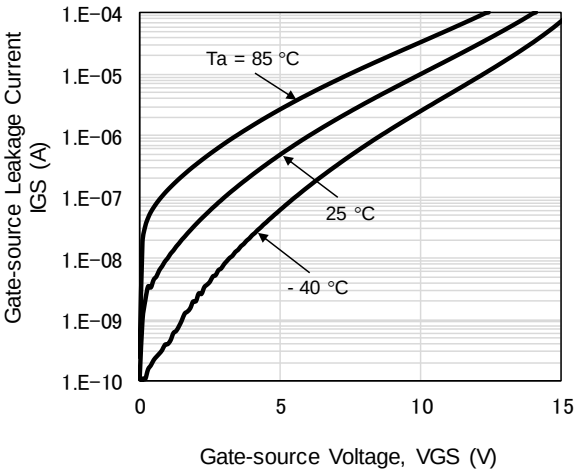
RSS(on) - VGS *1



IF - VF(s-s) *1

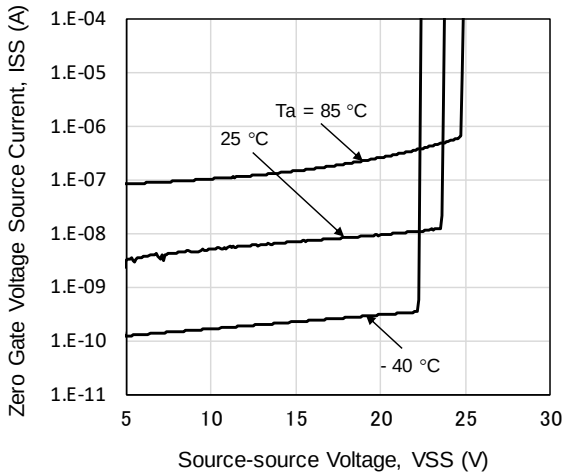


IGS - VGS *1

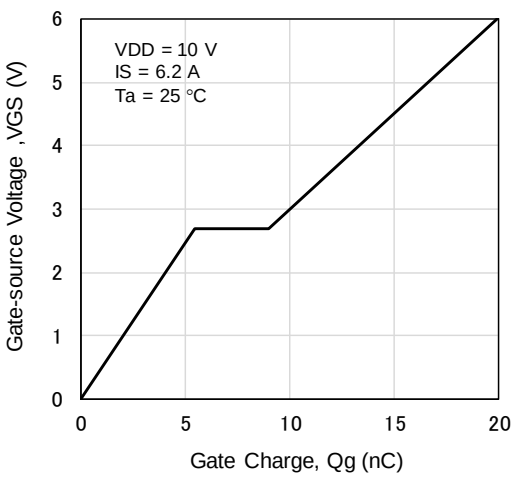


TECHNICAL DATA (Reference)

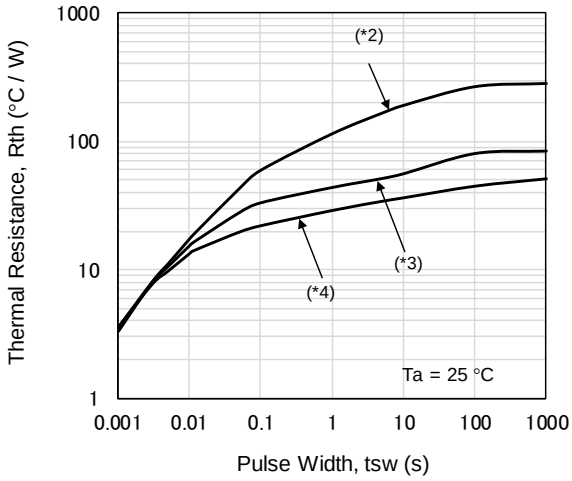
ISS - VSS *1



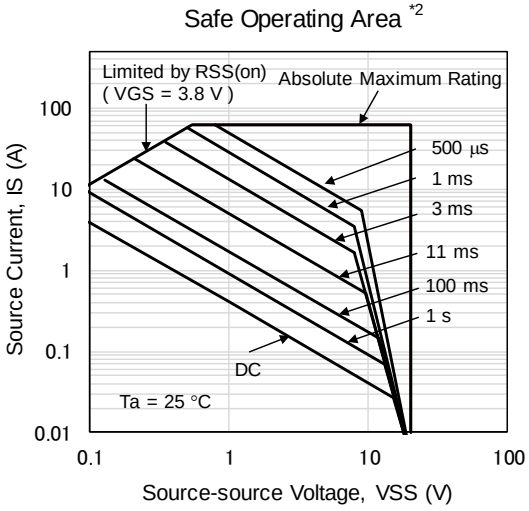
Dynamic Input / Output Characteristics



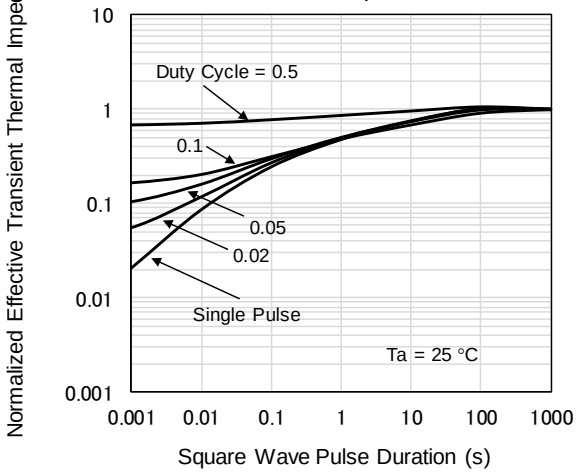
Rth - tsw



Safe Operating Area *2



Thermal Response *2



Note

*1 Pulse measurement.

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad
(30 mm^2 area, 36 µm thickness).

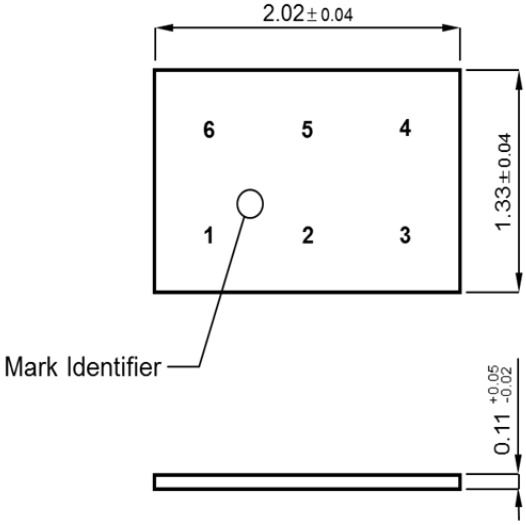
*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad
(610 mm^2 area, 36 µm thickness).

*4 Mounted on Ceramic board (70 mm x 70 mm x t1.0 mm).

9. OUTLINE

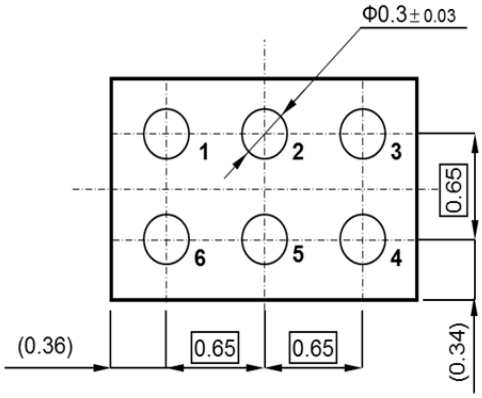
(Top View)

Unit: mm



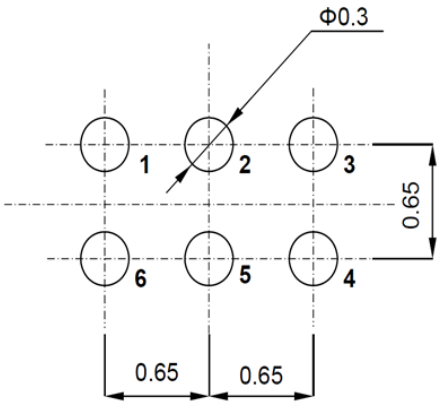
(Front View)

(Bottom View)



10. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.10.28	1.00	1. Initially issued.

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